A Study on Carbon Nano-Tube Field Effect Transistor (CNTFETs): A Promising Technology for future ICs

Ritambhara, Yazusha Sharma, Nishi Agarwal, Sandeep Vyas

Abstract—Presently, the low power and high efficiency are imperishable problem in technological gadgets. With the emergence of technologies like 5G and others, it has become requisite to meet the challenge before peeved. In this paper we entrust FinFETs, and CNTFETs technologies which are found to be upbeat field of research. The paper presents the performance enhancements of CNTFETs at 14 nm node and discusses the important areas of their applications and future scope.

Index Terms— CMOS, FinFETs, CNTFTs, Simulation, Permittivity, Device Modeling, Device Scalability, MOSFET, Scaling.

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1 INTRODUCTION

As Gordon Moore predicted, over the last three decades number of transistors in a single chip has been increased from thousand to several billion and suggested it doubles every year [1]. International Technology Roadmap for semiconductor in 2015 predicted and stated that in next five years CMOS technology will stop shrinking because industry will not able to scale CMOS resulting to death impart to Moore's law [2]. Si-MOSFET based technology has its own limitations like high power density, high leakage current, and decreased gate control resulting them to be inappropriate for ultra–high speed and low power applications. The limitations forced scientists and research to explore other alternatives, FinFETs and CNTFETs has emerged as most promising due to the properties like higher scalability, better performance and higher carrier mobility with suppressed short channel effect. Among the two alternatives CNTFETs are more preferred over FinFETs due to heat dissipation problem, as heat easily gets escalated on the fins. The Carbon the primary constituent of will surpass the silicon the widely employed material in the designing Integrated, Carbon will be the material for future integrated circuits [3],[4]. The advancements in technologies have resulted in high speed multi-core processors, memory storage with greater size and low power devices. Yet, today's devices based on robotics system, Artificial Intelligence and embedded systems demand higher speeds, much smaller sized IC's that what is being offered by existing technologies to push boundaries of their performance. To aid the development of such systems, it is necessary for IC technology to scale down the size of transistors and enhance the speed and performance with low power requirements. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) enabled to develop advanced systems like day to day required gadgets like Smart Phones, Laptops, etc., which is prior to the 22 nm node. With 22 nm node technology, further scaling down of MOSFET is not possible due to increased Short Channel Effects (SCE) such as Drain Induced Barrier lowering (DIBL), Impact Ionization, velocity saturation, Channel length modulation, so most of the foundries introduced new type of transistor called Fin Field Effect Transistor (FinFETs), which has less SCE's, and better control over the channel; this transistor structure is being used in 16 and 14 nm node also. The FinFETs based 14 nm node technology portrays some serious issues, which leads to the degraded performance of the ICs. The Technological advancements era had viewed other alternatives for MOSFET apart from FinFETs [5],[6] such as TFET[7], JLITFET[8] along with CNTFETs. Among all they will fail to compete with the CNTFET due to its advantages. As per the recommendation and credits by industry experts as well as researchers, CNTFET will be choice of next generation VLSI chips due to its small dimension and high performance [9],[10]. It has been reported that CNTFET based circuit are more efficient and 3 times faster than silicon based circuit at same power [11].

International Technology Road map for Semiconductors (ITRS) updates 2013 speaks that it is the future of transistors [12]. This paper is organized as follows; Section 2 presents FinFETs based device and their Issues and section 3 gives details about CNTFET technology and related issues. Sect 4 discusses the techniques for performance enhancement and various applications of CNTFETs are presented in section 5. The Section 6 covers the future scope with conclusion in last section.

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2. FINFETS DEVICE AND THEIR ISSUES:

In FinFETs both source and drain are connected with thin fin which forms the channel and the gate copes all around the channel to control current flow preciously; hence transistor entered into 3D form from the planar form [13]. Since more than one gate can be used to control the channel which in turn re-

duces leakage current and hence overcome the scaling issues. After a long time FinFETs was first implemented by Intel Corporation in 2011 by the name '3D Tri-Gate Transistor' in 22 nm process node [14]. FinFETs can be made in massive amount by extending bulk substrate as fin and using Shallow Trench Insulation (STI) and Silicon on Insulator (SOI) FinFETs by separate fin and substrate regions with oxide region in between them. FinFETs also can have different gating methods: double gate, tri-gate and gate-all-around. Tri-gate FinFETs are widely used by most of the industry and foundries due to their less additional cost and process simplicity [15]. Figure 1 depicts the structure of SOI-FinFETs with three gates. FinFETs suffers from disadvantages like heat dissipation through their fins due to vertical structure of its fin such as corner effects, parasitic capacitance and process-induced variability. Corner effects in FinFETs are caused due to their corners in rectangular fins of FinFETs which results in degraded performance. Parasitic capacitance include source and drain capacitance and capacitance that exist between two regions of FinFETs, which lead to poor performance and some reliability issues. Process induced variability includes Random Discrete Dopants (RDD) and Line Edge Roughness (LER). High temperature Ion Implantation Annealing process produces discrete dopants that are distributed randomly over the entire region causing RDD. FinFETs Technology provides numerous advantages over conventional CMOS such as higher speed, low power consumption, better mobility, high drive current and better scalability of transistor beyond 14nm technology.

3 .CNTFETs Devices and their Issues.

The first carbon nano- tube field effect transistor was reported in 1998. These were simple devices fabricated by depositing single wall CNTs the electrode serve as source and drain and connected via nano-tube channels and the doped Si- substrate served as the Gate. CNTFETs are promising and emerging nano-scale device for implementing very dense, low power and highly efficient circuits. CNTFETs uses semi-conducting material carbon in the form of carbon nano-tube as the channel [16]. The technology permits to have both n-channel and P-

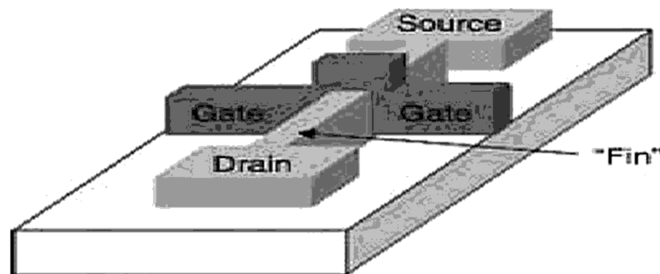
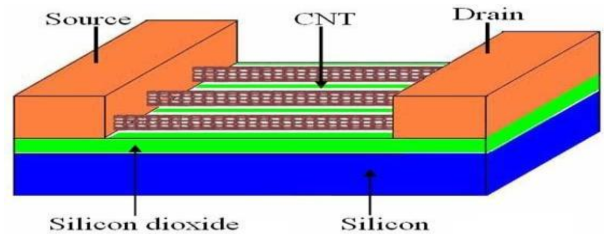


Fig:1 FinFETs structure with source, gate, drain and Fin region.[13]

channel devices from nano-tubes. In earlier developed CNTFETs were P- type with hole is the major carrier and carried the nomenclature Hole conductor CNTFETs. Unlike FinFET's, CNTFET's are ballistic devices which uses carbon instead of silicon with high mobility Carbon nano-tube (CNT) as channel. Ballistic regime is because of owing one dimension which greatly reduces the scattering probability. It has the ability to minimize sub-threshold slope and hence SCE's. Different types of CNTFET's are proposed since the invention of CNT's; such as MOSFET like CNTFET, Schottky barrier type CNTFET, surrounded gate CNTFET, suspended CNTFET, vertical CNTFET, etc. MOSFET like CNTFET has the advantages of CMOS process compatibility, less variation to changing gate length, high ON current, etc. When laying the nano-tube down upon the source and drain electrode posses' weak wander wall force for contact hence, the electrode were laid down on the top. In addition to carbon various other materials

Fig -2: Structure of CNFETs with gate, source Drain and Sub-



strate. [13]

like Au, Ti, Co were used to improve the metal/ nano-tube contact during annealing process, it is still in the research phase because of its reliability issues [11]. Another suggested design is -Surrounded gate CNTFET offering the advantage of better controllability over the channel. The challenges for its realization needs to address the issues such as controlling band gap energy, gate dielectric deposition, low resistance contact formation, placing of nano-tubes, etc. The structure of CNTFETs with Drain, Source, Gate and CNTs is shown in Fig-2.

Since half a decade, major advancements have been made in the fabrication of CNTFET's such as fabrication of carbon nano-tube computer with 178 transistors [9]. The standard parameters of the same are given in the Table-1 below.

Table-1 IRTS 2013 Standard Parameters for 22nm & 14nm Mode Technology

Device parameter Taken for simulation		
	Technology Modes	
Parameters	22nm	14nm
Channel Thickness (Lg) (nm)	22[20-25]	16.4
Oxide Thickness (Tox) (nm)	1	0.74
Fin Thickness (Tfin) (nm)	10[10-12]	6.2
Fin Height (Hfin) (nm)	40[30-50]	28[14-35]
Source drain Doping concentration	10^{10}	10^{10}
Channel doping concentration	10^{20}	10^{20}
Supply voltage	0.95	0.8

Our research work primarily focused on enhancing the performance of the FinFETs, using different techniques. we have completed the simulation in techniques suggested by ITRS update 2013. These techniques are described below:

DIFFERENT MODEL FOR CHANNEL

Silicon (Si) has less carrier mobility as compared to that of Germanium (Ge), Indium Gallium Arsenide (Inga As). As we know that the current in the device and carrier mobility are directly proportional to each other hence, it provides better performance. Ge is better option for channel but still have some issue in manufacturing. Hence, SiGe good candidate as channel.

HIGH K- MATERIAL AS INSULATOR

The concept of using high K dielectric material is already implemented in CMOS process. So the same concept of using high K- dielectric material is used here which enhance the performance of FinFETs [11].

IMPLEMENTATION OF GATE ALL AROUND STRUCTURE

Tri gate FinFETs are used to make ICs in many of the industry but when scaling them below 14nm their performance degrades because of increase in SCEs. Therefore ITRS 2013 update depicts that Implementation of gate all around is a solution of that using Si02 and Hf02 as gate dielectric.

4. RELATED WORK

As a device is scaled to their nano-size, it is quite difficult to model the device due to Quantum mechanics effect. Classical approach such as drift diffusion methods fails here. According to ITRS 13 update it is very difficult to model a device using Quantum Mechanical Approach using parameters at 14 nm technology or beyond. Firstly the simulation will be carried out for 22-nm node and then the same simulation process is again repeated for 14-nm node. Figure 3 shows the V-I characteristics of FinFETs in both technology nodes. It was observed that FinFETs will give more OFF current in 14-nm node without any additional performance enhancement technique. The increased OFF current of FinFETs in 14-nm can be easily inferred from the graph. ON current (ION), OFF cur- rent (IOFF) and ION/IOFF ratio of the FinFETs in all simulations are listed in Si and SiGe as the channel.

Table-2 : Comparison of FinFETs and CNTFETs with different Dielectric materials.

Result Comparison B/W FINFETs and CNTFETs with different Dielectric materials		
14nm Mode Technology	Ion/ I off ratio	
	FinFETs	CNTFETs
With low K di-electric material (Si02)	1.00E+03	5.25E+04
With high K di-electric material (Hf02)	4.40E+05	2.28E+06

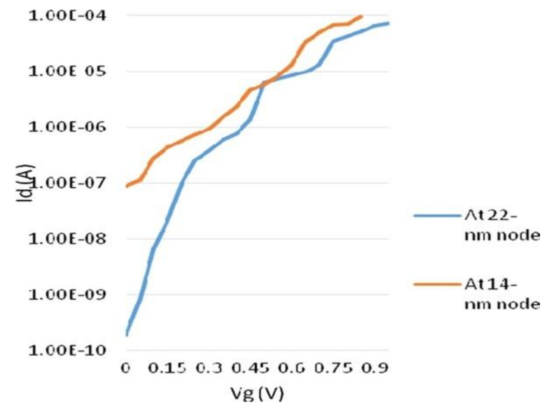


Fig. 3 V-I characteristics of FinFETs for 22-nm and 14-nm node [13]

V-I characteristics obtained from CNTFET simulation described in earlier section are shown in Fig. 4 for both 22-nm and 14-nm node. It is clearly indicated in the figure that CNTFET shows less variation in the performance as result of scaling. In this case use of High-k material (HfO2) dielectric will increase the ION/IOFF ratio. Finally results of FinFETs and CNTFETs simulation with different gate dielectrics are tabulated in the Table 2. It is clear from the table that CNTFETs shows better performance in comparison to that of FinFETs.

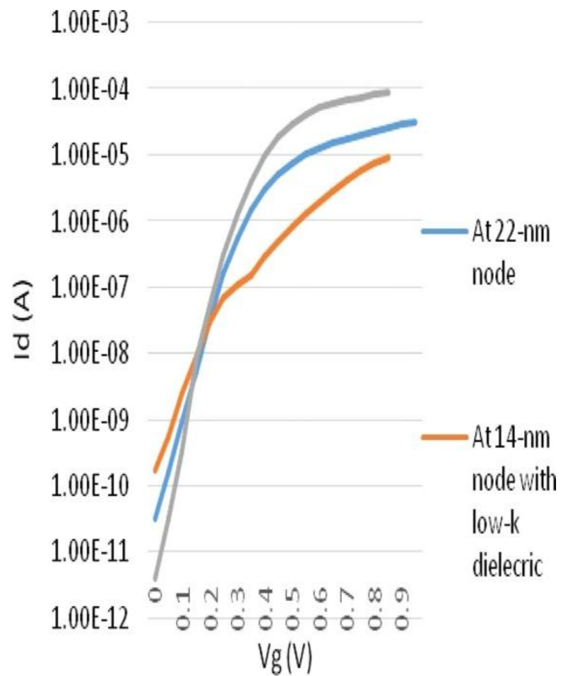


Fig. 4: V-I characteristics of CNTFETs in 22-nm and 14-nm[13]

6. Application of CNTFETs

As per literature survey, there are extensive applications of CNTFETs in varied fields. CNTFETs can be used as emerging candidate in numerous applications where MOSFETs are currently used. Hence Carbon is considered to surpass silicon in Integrated Circuits (ICs). CNTFETs device depict the similar character tics to that of Si based MOSFET nano-tube (CNTs) are recently considered an emerging block for future nano-electronics industry. Some of some possible application is listed below.

6.1. Communication Engineering

The linear relationship between applied voltage and drain current, CNTFETs finds their suitability for mobile communication system for incorporating several Complex Modulation Scheme [18].

6.2. RF and Microwave Applications:

R.F and Microwave are used in wireless remote control security and scan system to detect the image and location of buried object which compatible by wide variety of CNTFETs graphene FETs (GFETs) for the development of biosensor and Integrated on-chip security system with high sensitivity [4],[19],[20].

6.3. Bio-Medical Technology

Nowadays VLSI is widely used for implementing various biomedical applications to increase monitoring and diagnosis in healthcare. IOT based wearable devices and hearing aids, pacemakers are widely employed to improve the life span of human beings. These device Consist of various sensors based circuits which can be developed with Carbon nano-tube Field effect transistor (CNTFETs) instead of presently employed MOSFETs [21-25].

7. Future work.

It has been stated above that device modeling can be accurately done using quantum simulation; hence simulating the FinFETs and CNTFETs with quantum transport approach will lead to better and accurate results. Further, FinFETs variability analysis can also be done to understand the design issues in detail. Further, simulation for node less than 14-nm can also be performed for more research on FinFETs and CNTFET. Novel design methodologies with novel circuit are need of the hour to enhance the speed, reduce power consumption delay and area of CNTFETs with their fault tolerance detection at architectural level of design.

REFRENCES

[1] Moore Gordon E. Cramming more components onto integrated cir cuits. Electronics 1965;38(8):1
[2]http://spectrum.ieee.org/techtalk/computing/hardware/transistors-will-stop- shrinking-in-2021-moores-law-roadmap-predicts).
[3] Usmani FA, Hasan M (2010) Carbon nano-tube field effect transistors for high performance analog applications: an optimum design approach. Elsevier Micro electron J 41:395–402.
[4] Schröter Michael, Claus Martin, Sakalas Paulius, Haferlach M, Wang Dawei. Carbon nanotube FET technology for radio-frequency Electronics:
[5] Manoj CR, Ramgopal Rao V (2007) Impact of High-k gate dielectrics on the device and circuit performance of nanoscale FinFETs.
[6] Sloane N et al (2014) Random dopant, line-edge roughness, and gate work function variability in a nano InGaAs FinFET. IEEE Trans Electron Devices 61(2):466–472.
[7] Mishra Abhishek, ManishaPattanaik, Sharma Varun Gate Double. Vertical Tunnel FET for Hybrid CMOS-TFET based Low Standby Power Logic Circuits. International Conference on Microelectronics, Communication and Renewable Energy (ICMiCR-; 1-4; 2013.)
[8] Chiang Te-Kuang. A new threshold voltage model for short-channel junction less inverted T-shaped gate FETs (JLITFET). IEEE Trans Nanotechnology 2016 :15(3):442-7.
[9] Lubineau G, Mora A, Han F, Odeh IN, Yaldiz R. A morphological investigation of conductive networks in polymers loaded with carbon nanotubes. Computer Matter Sci 2017:130:21-38[Apr 1].
[10] Shreya Sonal, Chandel Rajeevan. Performance analysis of CNTFET based digital logic circuits. IEEE students conference on engineering and systems (SCES), 28–30 May, Allahabad; 2014. p. 1–6. 〈http://dx.doi.org/10.1109/SCES.2014.6880063〉.
[11] Bejenari Igor, Claus Martin. Electron back scattering in CNTFETs. IEEE Trans Electron Devices 2016;63(3):1340–50.
[12] ITRS (2013b) Process integration, devices, and structures, International Technology Roadmap for Semiconductors 2013 Edition.
[13] R.Hajare, C.lakshminaryana,G.H Ragunadana, Cyril prasama raj."Performance Enhancements of CNTFETs and FinFETs at different mode technologies", Vol-22, Issue-5, Publisher Springer Berlin Heidelberg, Page1121-1126.
[14] Sloane N et al (2014) Random dopant, line-edge roughness, and gate work function variability in a nano InGaAs FinFET. IEEE Trans Electron Devices 61(2):466–472.
[15] Shreya Sonal, Chandel Rajeevan. Performance analysis of CNTFET based digital logic circuits. IEEE students conference on engineering and systems (SCES), 28–30 May, Allahabad; 2014. p. 1–6. 〈http://dx.doi.org/10.1109/SCES.2014.6880063〉.
[16] Schröter Michael, Claus Martin, Sakalas Paulius, Haferlach M, Wang Dawei. Carbon nanotube FET technology for radio-frequency Electronics: state- of-the-art overview. IEEE J Electron Devices Soc 2013;1(1):9–20.
[17] Rispal Lorraine, Schwalke Udo. Structural and electrical characterization of carbon nanotube field-effect transistors fabricated by novel self-aligned growth method. In: Proceedings of the 3rd international conference on design and technology of in- targeted systems in nanoscale era, 2008. DTIS; 2008: 1-5.
[18] Farhana Soheli , Alam AHMZahirul , Khan Sheroz , Motakabber SMA . CNTFET spice model: design of a carbon nanotube field effect transistor. Proceedings of the 5th international conference on computer & communication engineering. 23-25 Sept, Kuala Lumpur; 2014. p. 262 – 4.
[19] Zhigang Xiao, John Elike, Alishia Reynolds, Roderick Moten, Xiang Zhao, The fabrication of carbon nanotube electronic circuits with dielectrophoresis; 2016.
[20] Schröter Michael, Claus Martin, Sakalas Paulius, Haferlach M, Wang

Dawei. Carbon nanotube FET technology for radio-frequency Electronics: state- of-the-art overview. IEEE J Electron Devices Soc 2013;1(1):9–20 .
[21] ⟨https://nano.stanford.edu/stanford-cnfet-model
[22] CNTFET for biomedical sensing application. IEEE international conference on advances in en gingering & technology research (ICAETR – 2014), August 01-02, Dr. Virendra Swarup Group of Institutions, Unnao, India; 1-4; 2014.
[23] h Jeseung, Yoo Gu, Chang Young Wook, Kim Hyung Joon, JoseO Joachim, Kim Eosu. Jae-ChulPyun, Kyung-HwaYoo. A carbon nanotube metal semiconductor field effect transistor-based biosensor for detection of amyloid-beta in human serum. Biosensor Bioelectron 2013;50:345-50.
[24] P.Bo] Zhu Z. An overview of carbon nanotubes and graphene for biosensing applications. Nano-Micro Lett 2017;9(3):25. [Jul 1].
[25]Ahmad Habib Muhammad Nazir , Jameel Kazi Muhammad , Islam Mohammad Shafquatul . Design and analysis of a CNTFET-based potentiostat ndavalli, LGorintin, F.Longnos, G.Feugens "Highly selective CNTFETs based sensor using diversification methods" proceeding volume 8101, Carbon nanotube Graphene, and Associated device 4: 8010A(2011).

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